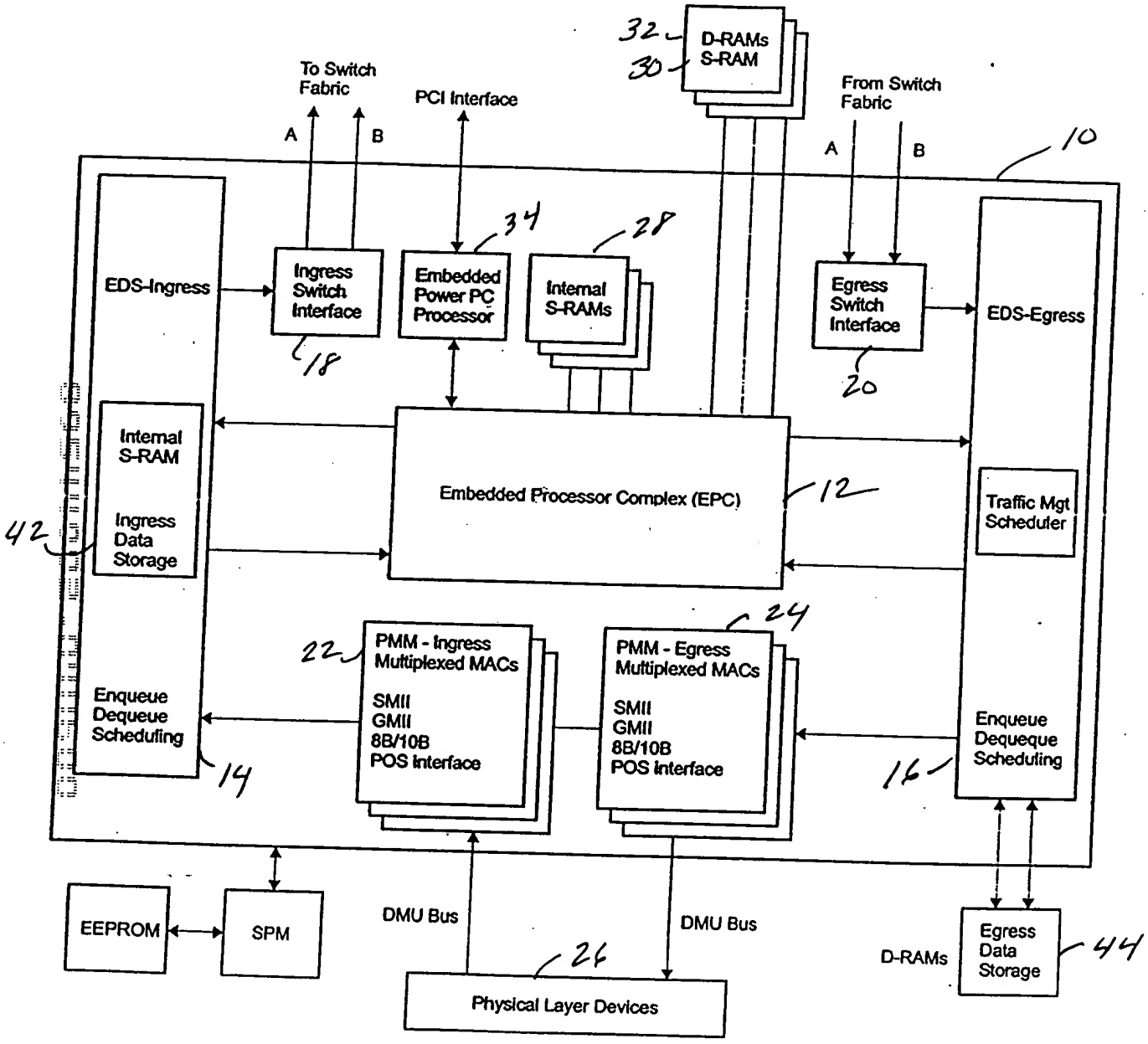
32
D-RAMs
S-RAM
30
To Switch Fabric
A
B
PCI Interface
From Switch Fabric
A
B
10
EDS-Ingress
Ingress Switch Interface
18
Embedded Power PC Processor
34
Internal S-RAMs
28
Egress Switch Interface
20
EDS-Egress
Internal S-RAM
Ingress Data Storage
42
Embedded Processor Complex (EPC)
12
Traffic Mgt Scheduler
22
PMM - Ingress Multiplexed MACs
SMII
GMII
8B/10B
POS Interface
24
PMM - Egress Multiplexed MACs
SMII
GMII
8B/10B
POS Interface
Enqueue Dequeue Scheduling
14
Enqueue Dequeque Scheduling
16
EEPROM
SPM
DMU Bus
DMU Bus
26
Physical Layer Devices
D-RAMs
Egress Data Storage
44

FIG. 1

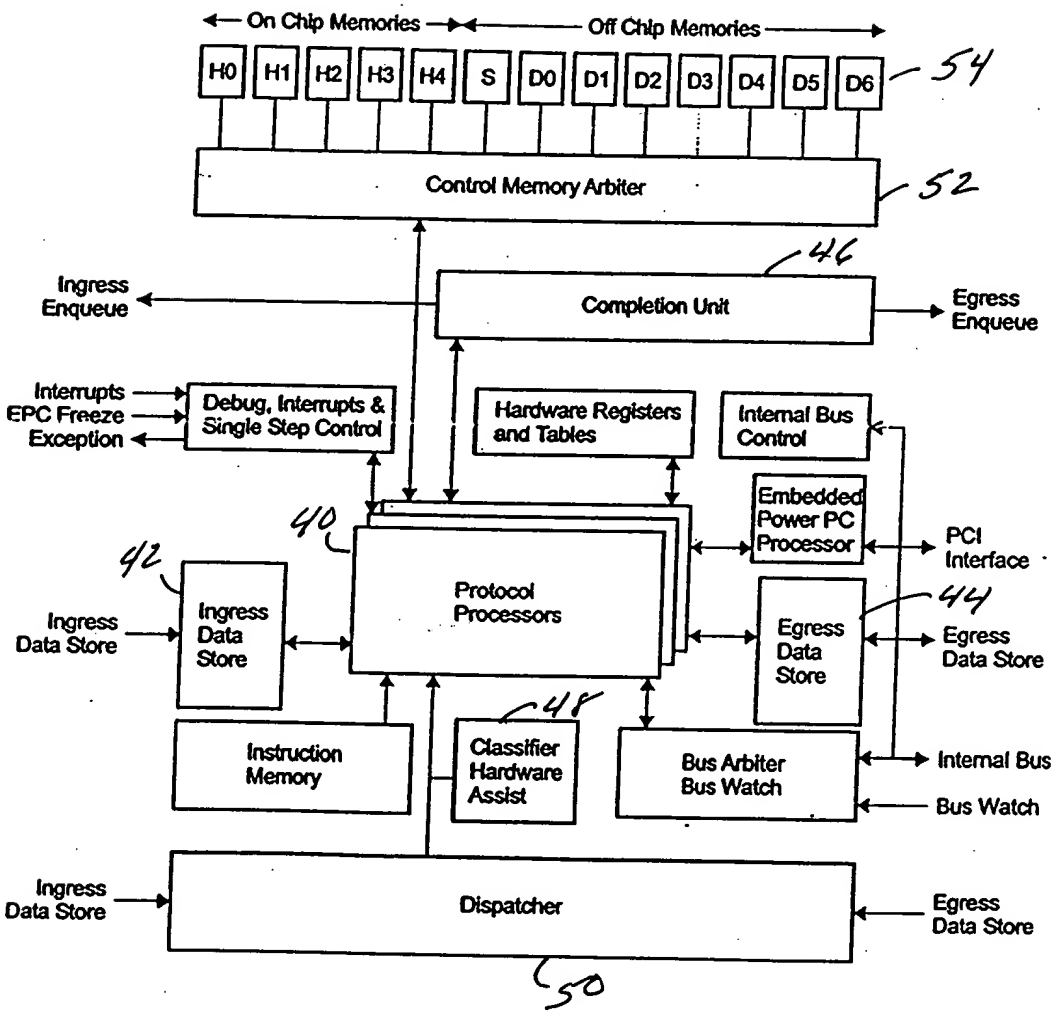
On Chip Memories
Off Chip Memories
H0
H1
H2
H3
H4
S
D0
D1
D2
D3
D4
D5
D6
54
Control Memory Arbiter
52
46
Ingress Enqueue
Completion Unit
Egress Enqueue
Interrupts
EPC Freeze
Exception
Debug, Interrupts & Single Step Control
Hardware Registers and Tables
Internal Bus Control
Embedded Power PC Processor
PCI Interface
40
42
Ingress Data Store
Ingress Data Store
Protocol Processors
44
Egress Data Store
Egress Data Store
48
Instruction Memory
Classifier Hardware Assist
Bus Arbiter Bus Watch
Internal Bus
Bus Watch
Ingress Data Store
Dispatcher
Egress Data Store
50

FIG. 2

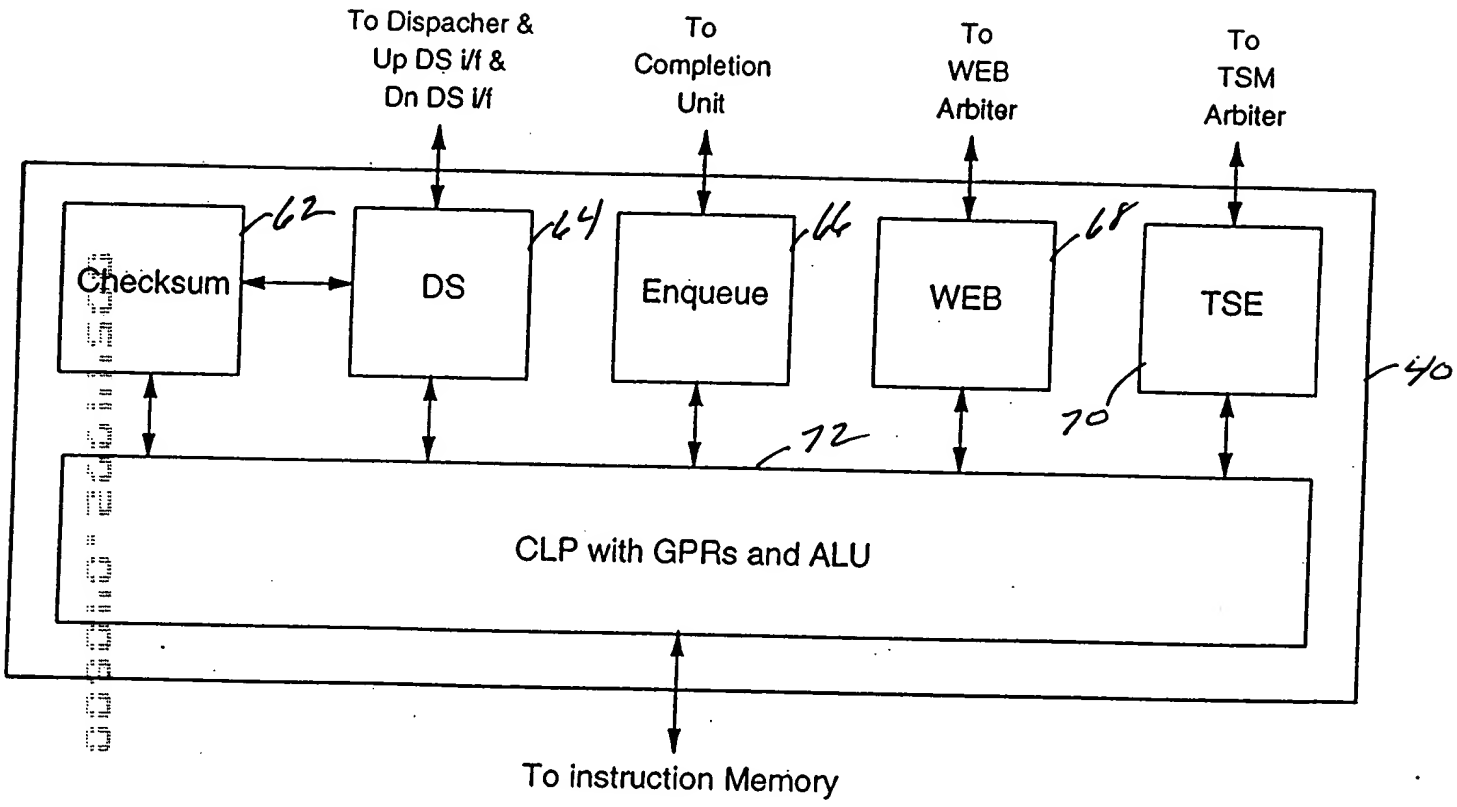
To Dispacher & Up DS i/f & Dn DS i/f
To Completion Unit
To WEB Arbiter
To TSM Arbiter
Checksum
62
DS
64
Enqueue
66
WEB
68
TSE
70
40
72
CLP with GPRs and ALU
To instruction Memory

FIG. 3

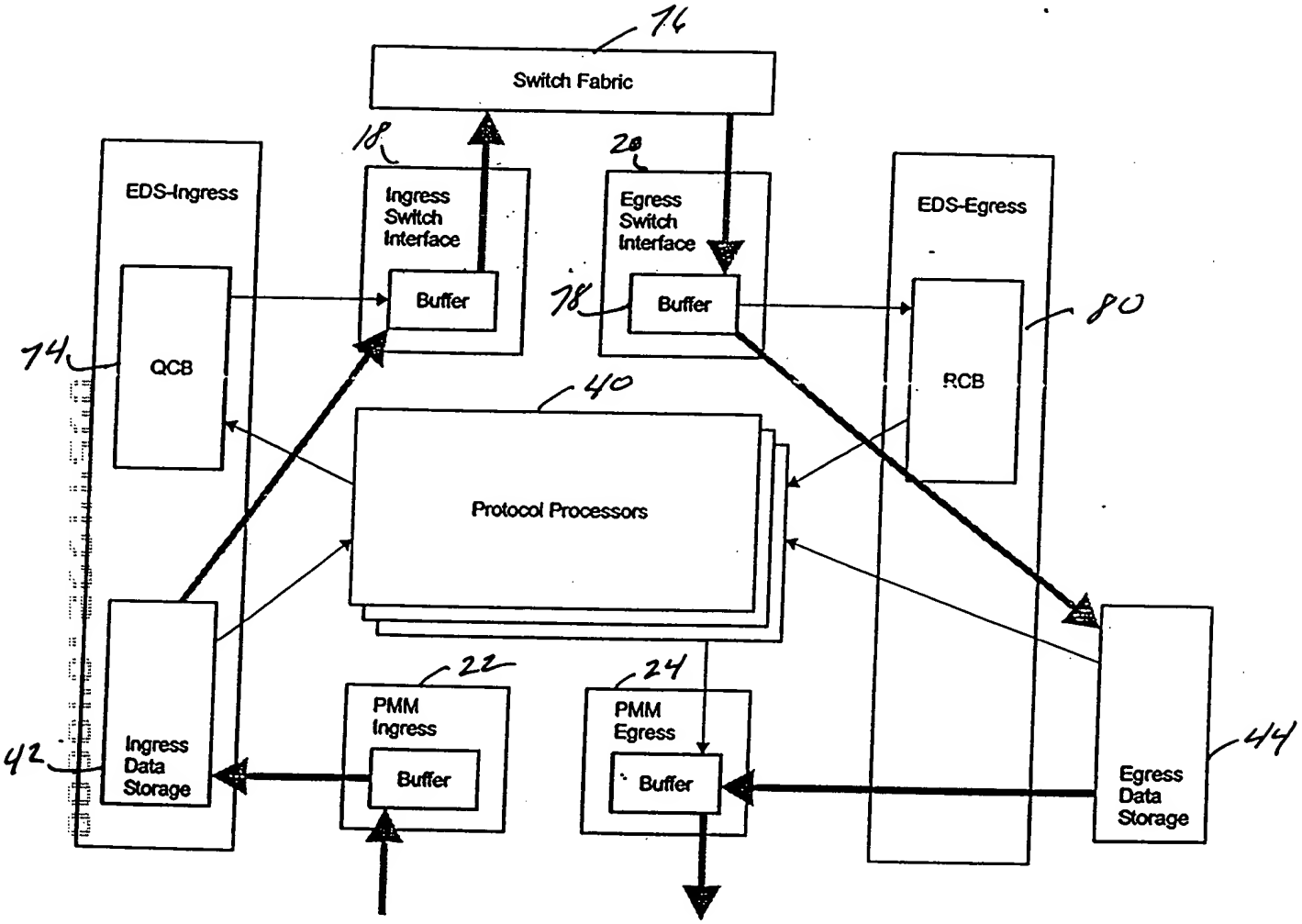
76
Switch Fabric
18
20
EDS-Ingress
Ingress Switch Interface
Buffer
Egress Switch Interface
Buffer
EDS-Egress
74
QCB
78
80
RCB
40
Protocol Processors
22
24
PMM Ingress
Buffer
PMM Egress
Buffer
42
Ingress Data Storage
Egress Data Storage
44

FIG. 4

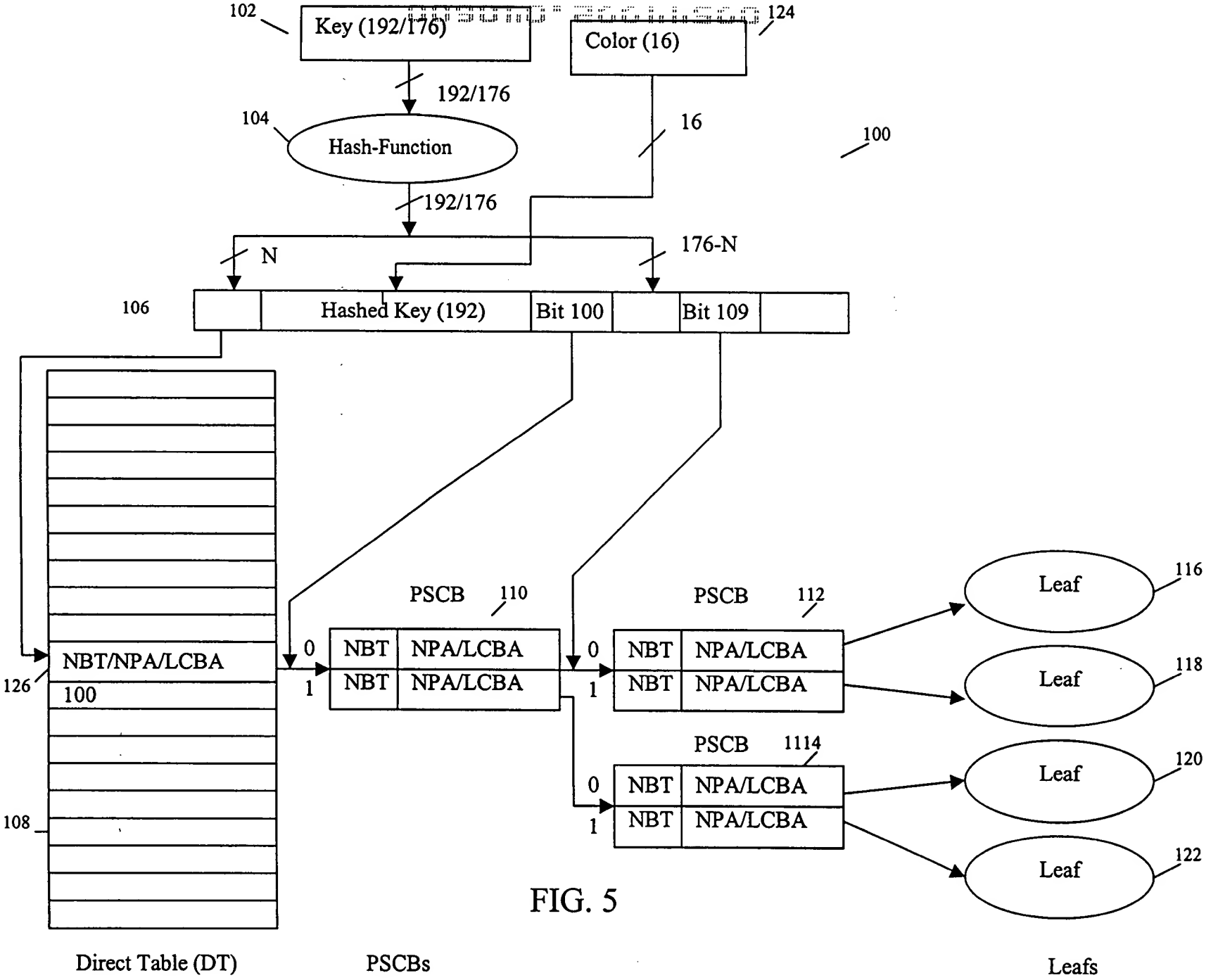

FIG. 5

RAL9-1999-0140-US1
Basset al
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RAL9-1999-0110-US1
Bass et al
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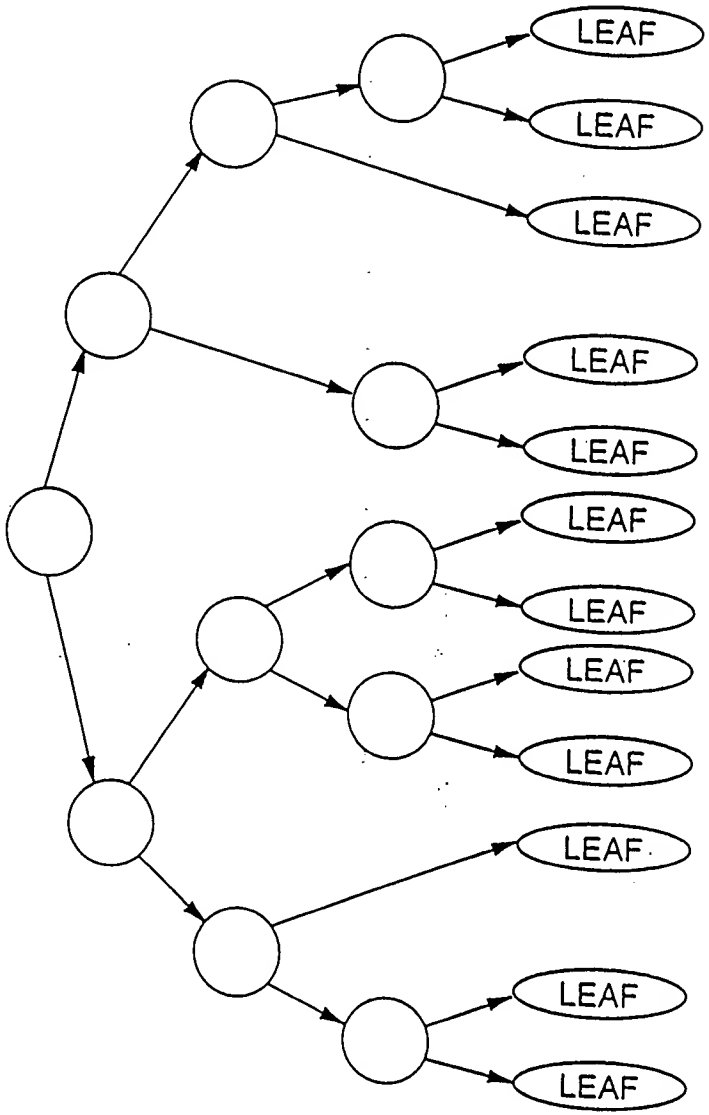
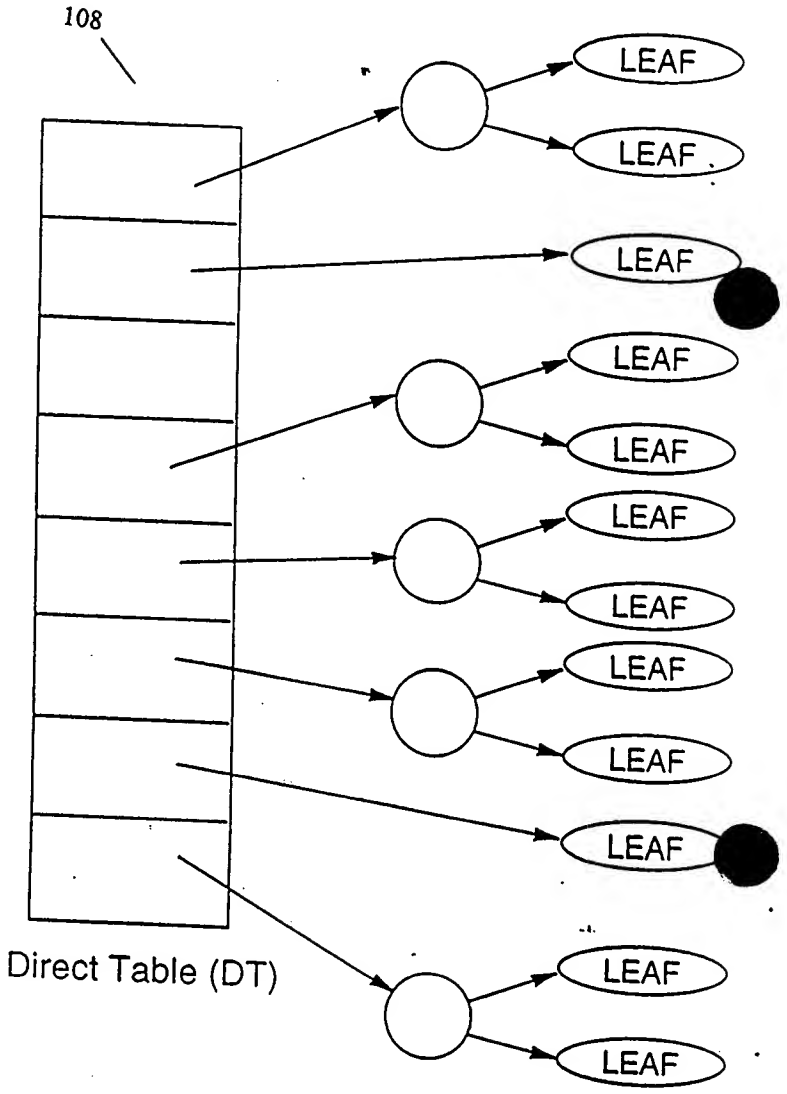


Datastructure without using a Direct Table



Datastructure with using a Direct Table

FIG. 6

RAL-1999-0140-US1
Bass et al
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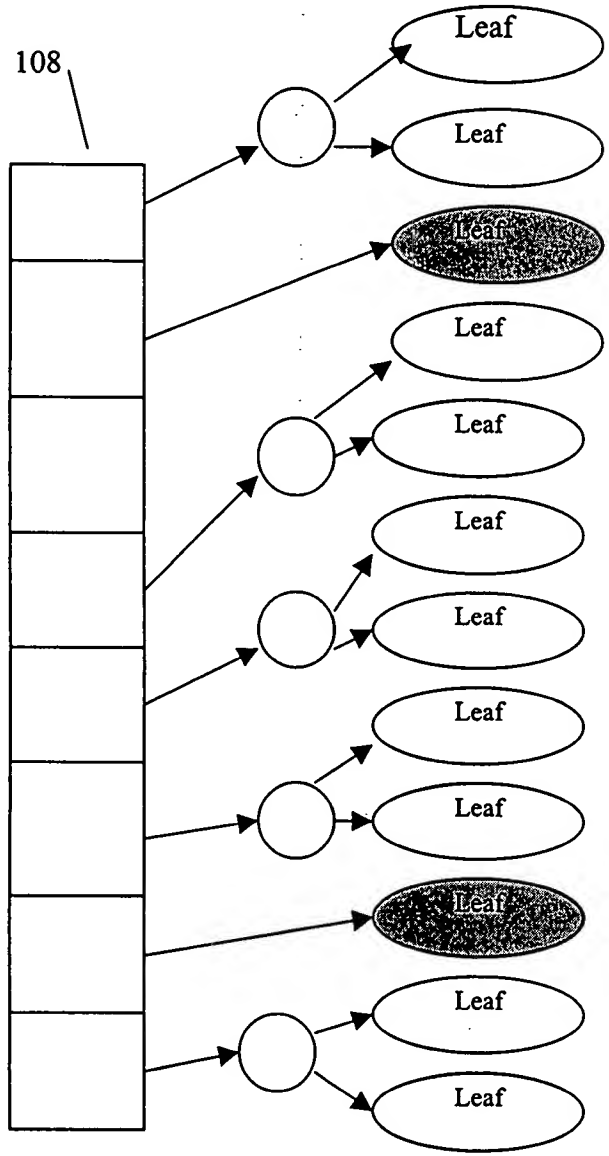
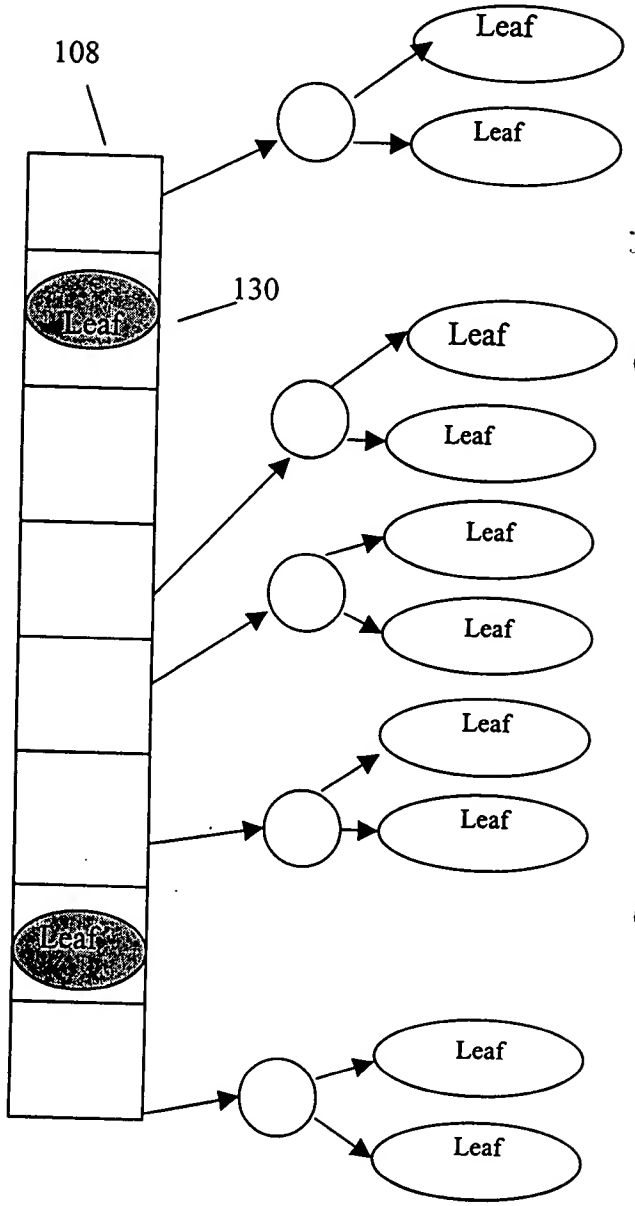


Datastructure without Direct Leaves

FIG. 7



Datastructure with Direct Leaves

RAL9-1999-0140-US1
Bass et al
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Format	Conditions	Valid in DTEntry?	Valid in PSCB?	Format (2 bits)	NPA (26 bits)	NBT (8 bits)	LCBA (26 bits)	Spare (2 bits)
Empty DTEntry	No leaves	Yes	Yes	00	0	0	0	0
LCBA not valid	DTEntry contains pointer to PSCB	Yes	Yes	00	NPA	NBT	0	0
LCBA valid; NPA/NBT not valid	Single leaf associated with DTEntry; LCBA contains pointer into leaf; No pointer to next PSCB	Yes	Yes	01	0	0	LCBA	0
LCBA valid; NPA/NBT valid	Single leaf associated with DTEntry; LCBA contains pointer to leaf; Pointer to next PSCB	Yes	Yes	01	NPA	NBT	LCBA	0

FIG. 8

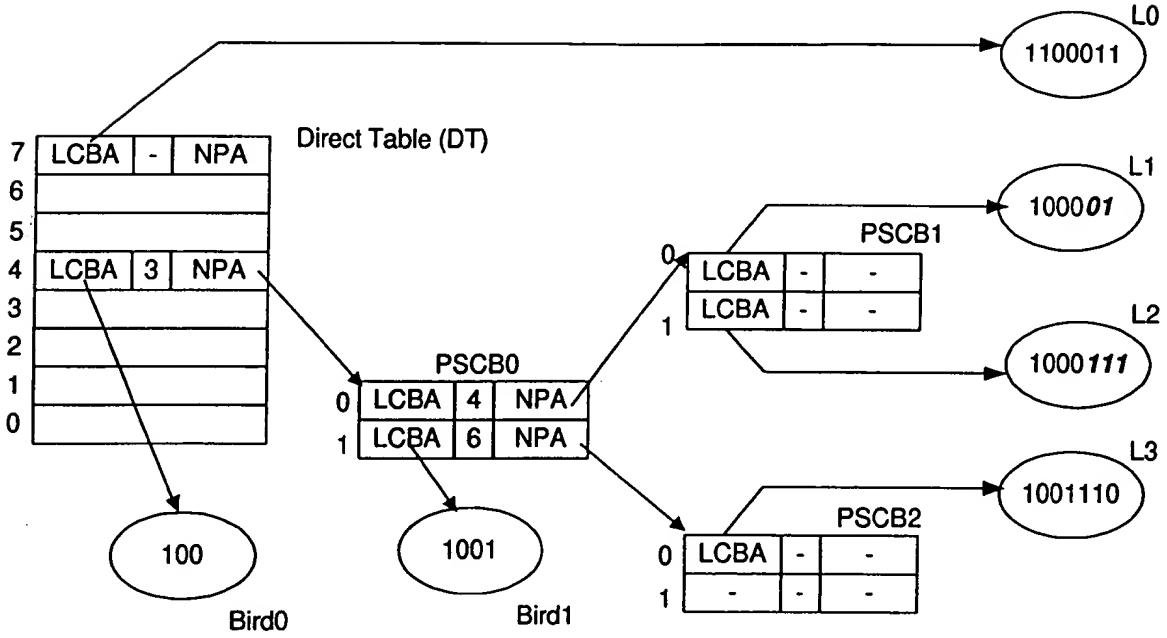

FIG. 9

Input Key	Input Key Length	Pattern stored in the leaf	Leaf-pattern Length	DISP
10011	5	1011010	7	2
10011	5	1001101	7	5
1011010	7	10011	5	2

FIG. 10

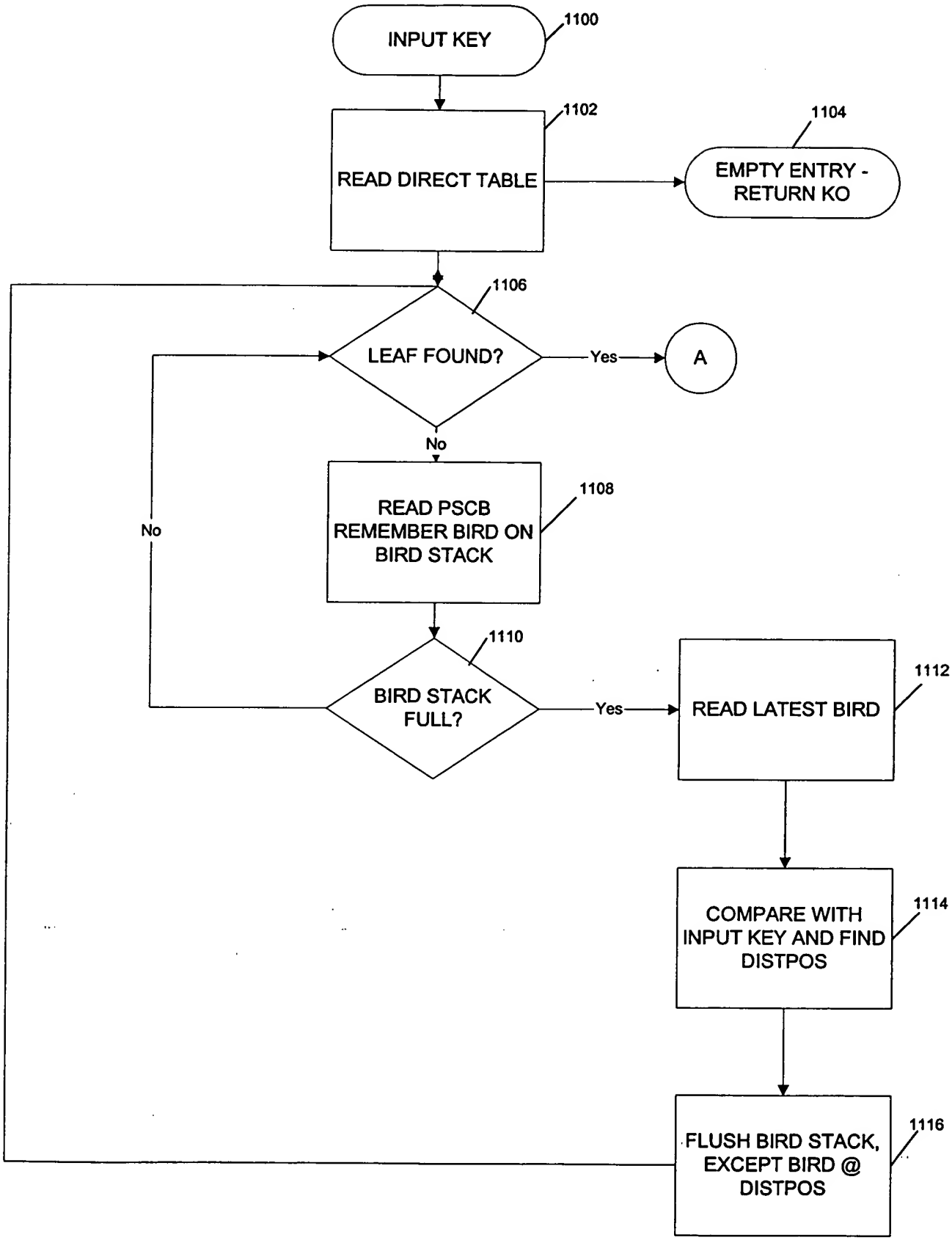
INPUT KEY
1100
READ DIRECT TABLE
1102
EMPTY ENTRY - RETURN KO
1104
LEAF FOUND?
1106
Yes
A
No
READ PSCB REMEMBER BIRD ON BIRD STACK
1108
No
BIRD STACK FULL?
1110
Yes
READ LATEST BIRD
1112
COMPARE WITH INPUT KEY AND FIND DISTPOS
1114
FLUSH BIRD STACK, EXCEPT BIRD @ DISTPOS
1116

FIG. 11A

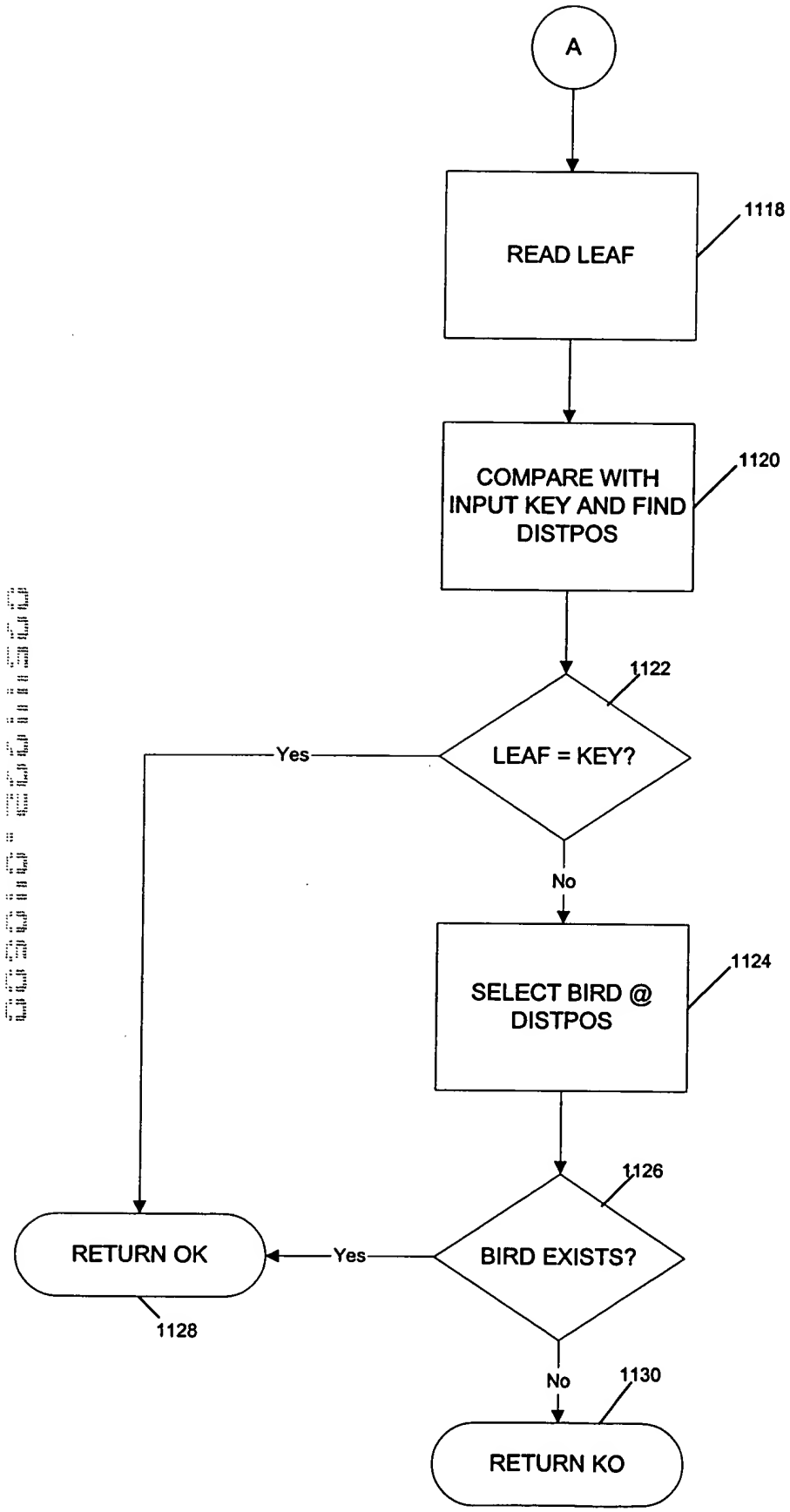
A
READ LEAF
1118
COMPARE WITH INPUT KEY AND FIND DISTPOS
1120
1122
LEAF = KEY?
Yes
No
SELECT BIRD @ DISTPOS
1124
1126
BIRD EXISTS?
Yes
RETURN OK
1128
No
1130
RETURN KO

FIG. 11B

LUDefTable Tree Definition

Field	Size	Bits
CacheEntry	1	0
Tree_Type	2	2..1
hash-type	4	6..3
color_en	1	7
PIP2_max_size	5	12 .. 8
NPARope_en	1	13
NPASMT_en	1	14
CompIndex_en	1	15
PSCB_fq_index	6	21 .. 16
PSCB_Height	1	22
Mask_Vector_En	1	23
CompIndex	8	31..24
DT_base_addr	26	57 .. 32
DT_size	4	61 .. 58
DT_interleaf	2	63 .. 62
Leaf_fq_index	6	69 .. 64
Leaf_Width	2	71 .. 70
Leaf_Height	3	74 .. 72
DirectLeafEn	1	75

FIG. 12

Field	Size	Address in TSM where PSCB is located
NPA0	26	Next PSCB address: pointer to next PSCB in the tree for 0-part of PSCB
NBT0	8	Next bit to test for 0-part of PSCB
LCBA0	26	Leaf control block address: pointer to leaf for 0-part of PSCB
NPA1	26	Next PSCB address: pointer to next PSCB in the tree for 1-part of PSCB
NBT1	8	Next bit to test for 1-part of PSCB
LCBA1	26	Leaf control block address: pointer to leaf for 1-part of PSCB
Index	8	Index of this PSCB (physically stored in the previous PSCB)
PatBit	1	The value of HashedKey[Index], based on the value of the Index field in the PSCB register

FIG. 13

Field Name	Length	Description
NLARope	4 bytes	Leaf Chaining Pointer, aging information and direct leaf information
Prefix_Len	1 byte	The length of the pattern *minus 1* (in bits) for LPM
pattern	2 - 18 bytes	Pattern to be compared with the HashedKey
UserData	Variable	The contents of this field is under complete picocode control; the UserData field can include one or more counters

FIG. 14

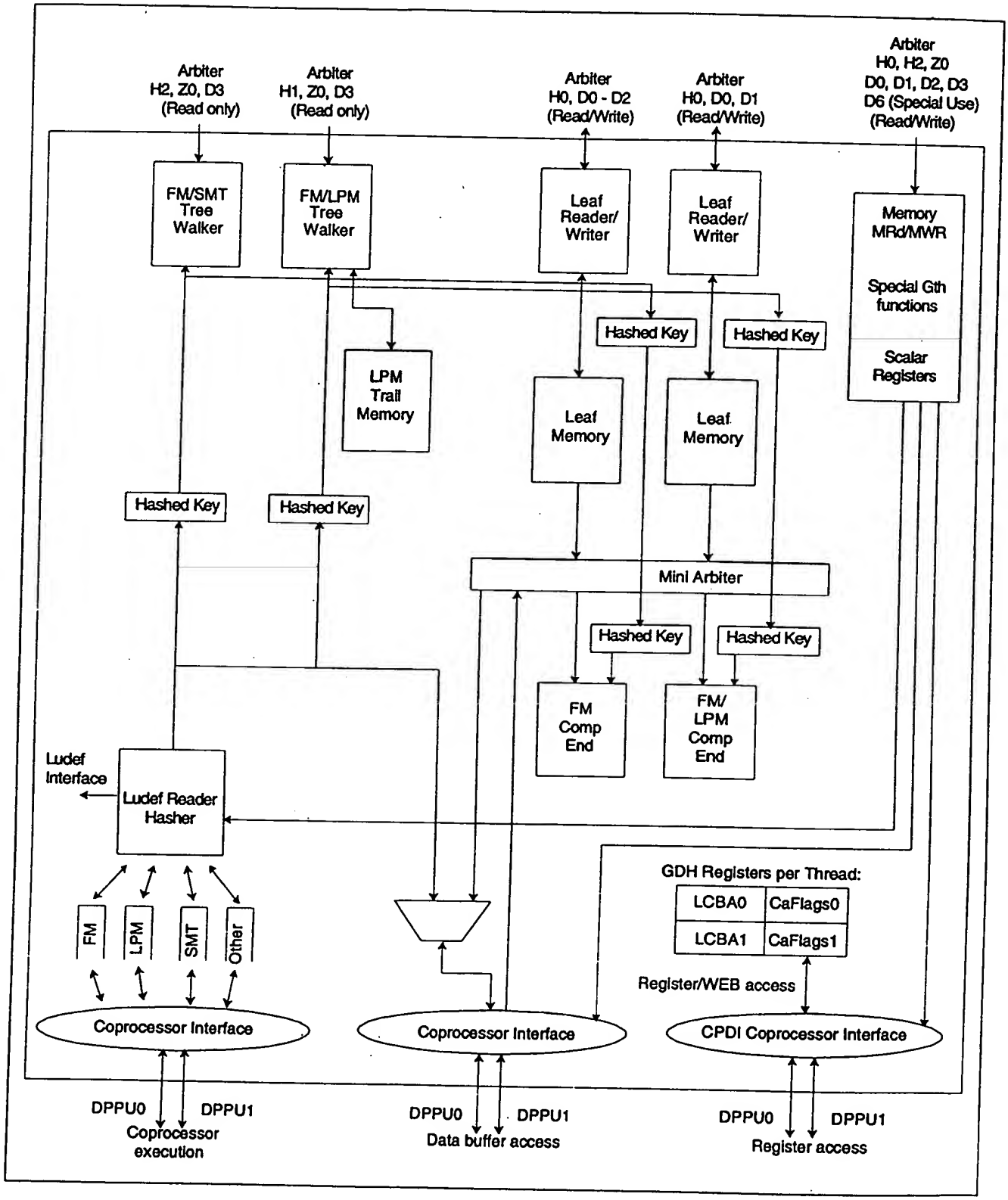
Arbiter
H2, Z0, D3
(Read only)
Arbiter
H1, Z0, D3
(Read only)
Arbiter
H0, D0 - D2
(Read/Write)
Arbiter
H0, D0, D1
(Read/Write)
Arbiter
H0, H2, Z0
D0, D1, D2, D3
D6 (Special Use)
(Read/Write)
FM/SMT Tree Walker
FM/LPM Tree Walker
Leaf Reader/ Writer
Leaf Reader/ Writer
Memory MRd/MWR
Special Gth functions
Scalar Registers
Hashed Key
Hashed Key
LPM Trail Memory
Leaf Memory
Leaf Memory
Hashed Key
Hashed Key
Mini Arbiter
Hashed Key
Hashed Key
FM Comp End
FM/ LPM Comp End
Ludef Interface
Ludef Reader Hasher
FM
LPM
SMT
Other
GDH Registers per Thread:
LCBA0
CaFlags0
LCBA1
CaFlags1
Register/WEB access
Coprocessor Interface
Coprocessor Interface
CPDI Coprocessor Interface
DPPU0
DPPU1
Coprocessor execution
DPPU0
DPPU1
Data buffer access
DPPU0
DPPU1
Register access

FIG. 15